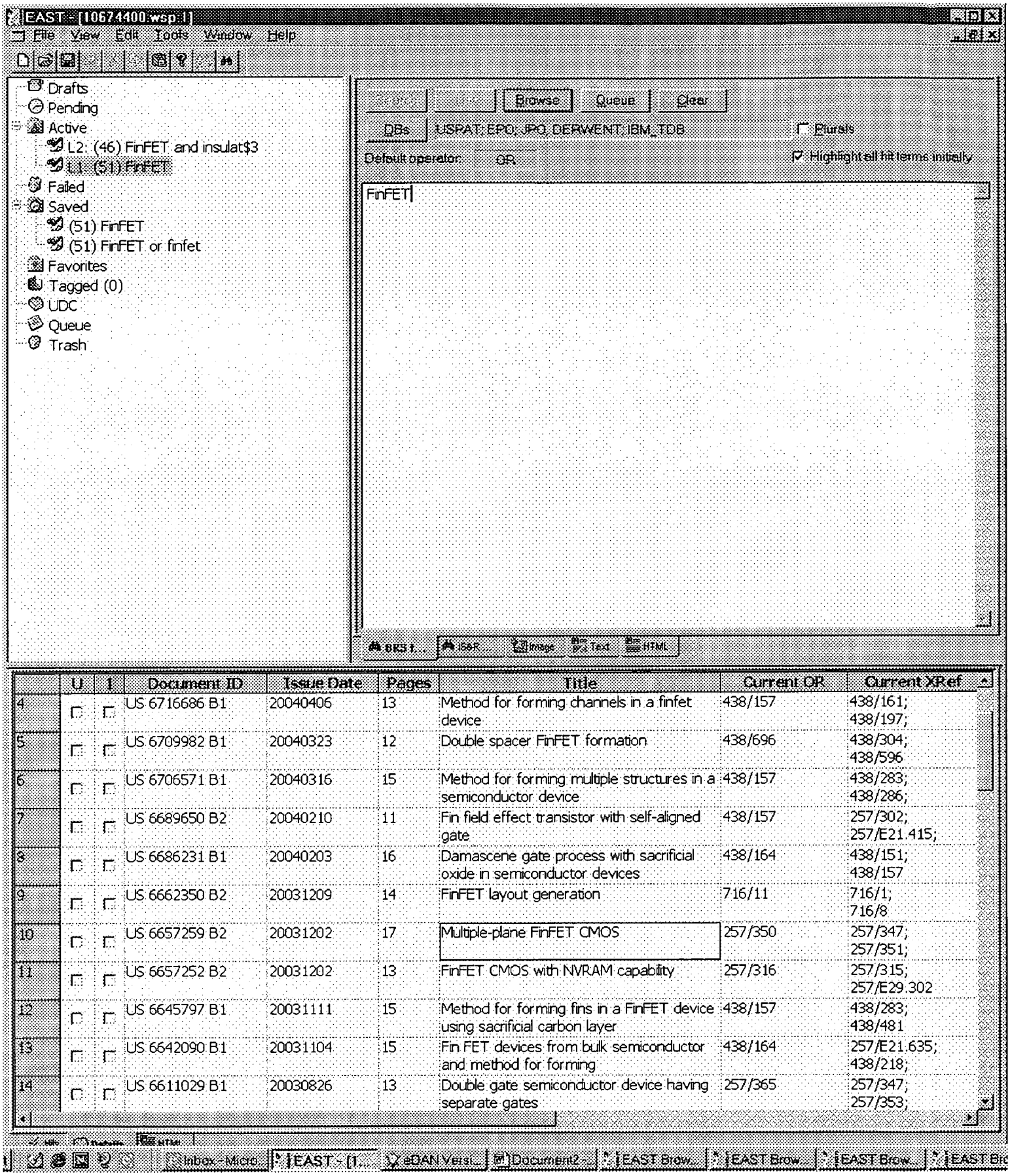

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
4	☐	☐	US 6716686 B1	20040406	13	Method for forming channels in a finfet device	438/157	438/161; 438/197;
5	☐	☐	US 6709982 B1	20040323	12	Double spacer FinFET formation	438/696	438/304; 438/596
6	☐	☐	US 6706571 B1	20040316	15	Method for forming multiple structures in a semiconductor device	438/157	438/283; 438/286;
7	☐	☐	US 6689650 B2	20040210	11	Fin field effect transistor with self-aligned gate	438/157	257/302; 257/E21.415;
8	☐	☐	US 6686231 B1	20040203	16	Damascene gate process with sacrificial oxide in semiconductor devices	438/164	438/151; 438/157
9	☐	☐	US 6662350 B2	20031209	14	FinFET layout generation	716/11	716/1; 716/8
10	☐	☐	US 6657259 B2	20031202	17	Multiple-plane FinFET CMOS	257/350	257/347; 257/351;
11	☐	☐	US 6657252 B2	20031202	13	FinFET CMOS with NVRAM capability	257/316	257/315; 257/E29.302
12	☐	☐	US 6645797 B1	20031111	15	Method for forming fins in a FinFET device using sacrificial carbon layer	438/157	438/283; 438/481
13	☐	☐	US 6642090 B1	20031104	15	Fin FET devices from bulk semiconductor and method for forming	438/164	257/E21.635; 438/218;
14	☐	☐	US 6611029 B1	20030826	13	Double gate semiconductor device having separate gates	257/365	257/347; 257/353;